WHAT IS CLAIMED IS:

1. An apparatus comprising a transistor configured to store data, wherein:

a gate of the transistor is configured to receive a first control signal;

a first channel interface of the transistor is configured to receive a data signal; and

a second channel interface of the transistor is configured to receive a second control signal.

2. The apparatus of claim 1, wherein the apparatus is a memory device.

3. The apparatus of claim 2, wherein the memory device is a dynamic random access memory device.

4. The apparatus of claim 3, wherein the dynamic random access memory device is a floating body dynamic random access memory device.

5. The apparatus of claim 1, wherein the transistor is a floating body transistor.

6. The apparatus of claim 1, wherein:

the first channel interface is a drain; and

the second channel interface is a source.

7. The apparatus of claim 1, wherein:

the first channel interface is a source; and

the second channel interface is a drain.

8. The apparatus of claim 1, wherein a word line is coupled to the gate of the transistor.

9. The apparatus of claim 1, wherein a bit line is coupled to the first channel interface of the transistor.

10. The apparatus of claim 2, wherein a purge line is coupled to the second channel interface of the transistor.

11. The apparatus of claim 1, wherein the apparatus is configured to write data to the transistor by resetting a floating body of the transistor and then writing data to the floating body of the transistor.

12. The apparatus of claim 11, wherein said resetting the floating body of the transistor comprises receiving a first voltage level at the second channel interface of the transistor.

13. The apparatus of claim 12, wherein the first voltage level is part of the second control signal.

14. The apparatus of claim 12, wherein the first voltage level is in a range of -0.5V to -2.5V.

15. The apparatus of claim 12, wherein said resetting the floating body of the transistor comprises receiving a second voltage level at the gate of the transistor.

16. The apparatus of claim 15, wherein the second voltage level is part of the first control signal.

17. The apparatus of claim 15, wherein the second voltage level is in a range of -.5V to -2.5V.

18. The apparatus of claim 15, wherein the first voltage level and the second voltage level are received at the transistor overlapping in time.

19. The apparatus of claim 11, wherein said writing data to the floating body of the transistor comprises receiving a third voltage level at the first channel interface of the transistor.

20. The apparatus of claim 19, wherein the third voltage level is part of the data signal.

21. The apparatus of claim 19, wherein:

the third voltage level is approximately 0V if data written to the transistor represents a logical 0; and

the third voltage level is in a range of 0.5V to 2.5V if data written to the transistor represents a logical 1.

22. The apparatus of claim 19, wherein said writing data to the floating body of the transistor comprises:

receiving a fourth voltage level at the second channel interface of the transistor; and

receiving a fifth voltage level at the gate of the transistor.

23. The apparatus of claim 22, wherein:

the fourth voltage level is part of the second control signal; and

the fifth voltage level is part of the first control signal.

24. The apparatus of claim 22, wherein the third voltage level, the fourth voltage level, and the fifth voltage level are received at the transistor overlapping in time.

25. The apparatus of claim 22, wherein the fourth voltage level is approximately –0.5V to 0V.

26. The apparatus of claim 22, wherein the fifth voltage level is in a range of 0.5V to 2.5V.

27. A method comprising:

resetting a floating body of the transistor with a first set of control signals overlapping in time; and

selectively writing data to the floating body of the transistor with a second set of control signals and a data signal overlapping in time.

28. The method of claim 27, wherein:

the first set of control signals and the second set of control signals are received at a gate of the transistor and a first channel interface of the transistor; and

the data signal is received at a second channel interface of the transistor.

29. A system comprising:

a die comprising a processor; and

an off-die component in communication with the processor;

wherein the processor comprises a transistor configured to store data, wherein:

a gate of the transistor is configured to receive a first control signal;

a first channel interface of the transistor is configured to receive a data signal; and

a second channel interface of the transistor is configured to receive a second control signal.

30. The system of claim 29, wherein the off-die component is at least one of a cache memory, a chip set, and a graphical interface.